Patent Search

Patents **1 - 10** of **35** on **evolvable circuit**. (**0.00** seconds)

Evolvable circuit with transistor-level reconfigurability
US Pat. 6728666 - Filed Sep 13, 1999 - The United States of America as represented by the Administrator of the National Aeronautics and Space Administration
Evolvable circuit ...

Method and apparatus for relocating elements in an **evolvable** configuration bitstream
US Pat. 6539532 - Filed Jun 17, 1999 - Xilinx, Inc.
Optionally insert 1 > test **circuit** ^ i Translate chromosome 1 306 into bitstream
... "**Evolvable** Hardware with Development", IEEE International Symposium on ...

Method and apparatus for testing **evolvable** configuration bitstreams
US Pat. 6363519 - Filed Jun 17, 1999 - Xilinx, Inc.
To prevent evolution of an asynchronous **circuit**, selected resources can be fixed or disabled ... At step 305, a test **circuit** is optionally inserted into the ...

Myoelectric-pattern classification method and apparatus
US Pat. 6859663 - Filed Jan 29, 2002 - National Institute of Advanced Industrial Science and Technology
In contrast to conventional hardware where the **circuit** structure is fixed in the design process, the feature of this **evolvable** chip is that it is designed ...

Timing adjustment of clock signals in a digital **circuit**
US Pat. 6658581 - Filed Mar 6, 2000 - Agency of Industrial Science & Technology
(54) TIMING ADJUSTMENT OF CLOCK SIGNALS IN A DIGITAL **CIRCUIT** (75) Inventors: Eiichi Takahashi, ... Tokyo (JP); **Evolvable** System Research Institute, Inc., ...

Evolutionary technique for automated synthesis of electronic circuits
US Pat. 6526556 - Filed Jun 7, 2000 - The United States of America as represented by the Administrator of the National Aeronautics and Space Administration
Zebulum et al, "**Evolvable** Hardware: on the Automatic Synthesis of Analog Control Systems," IEEE ... Adrian Stoica, "**Evolvable** Hardware: From on-Chip **Circuit** ...

System and method for coevolutionary **circuit** design
US Pat. 6889366 - Filed Dec 27, 2001 - LSI Logic Corporation
X. Yao, Following the Path of **Evolvable** Hardware, Com-munications of the ACM, ... A system suitable for provid-ing integrated **circuit** design may include a ...

Evolved circuits for bitstream protection
US Pat. 6894527 - Filed May 12, 2003 - Xilinx, Inc.
al., "On **Evolvable** Hardware,"5o/r Computing in Industrial Electronics, 2002, pp. ... The security **circuit** can be a decryption and/or encryption **circuit** that ...

Evolutionary technique for automated synthesis of electronic circuits
US Pat. 7072814 - Filed Jan 29, 2002 - The United States of America as represented by the Administrator of the National Aeronautics and Space Administration
Pairing of the transistors, however, is expected to provide a universal application for an **evolvable** analog **circuit**. Similarly, arranging the transistors in ...

Method and apparatus for automatic synthesis, placement and routing of complex structures

US Pat. 6424959 - Filed Jun 17, 1999 - John R. Koza
The netlist for a **circuit** is a list that identifies each component of the **circuit**, the nodes to which ... **circuit** by embedding it in **evolvable** hardware, ...

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Patent Search

Patents **1** - **10** of **47** on **evolvable logic**. (**0.00** seconds)

Method and apparatus for relocating elements in an **evolvable** configuration bitstream
US Pat. 6539532 - Filed Jun 17, 1999 - Xilinx, Inc.
area of the programmable **logic** device; means for creating respective ...
Other chromosomes and other non-**evolvable logic** may also be incorporated in a ...

Method and apparatus for testing **evolvable** configuration bitstreams
US Pat. 6363519 - Filed Jun 17, 1999 - Xilinx, Inc.
(54) METHOD AND APPARATUS FOR TESTING **EVOLVABLE** CONFIGURATION BITSTREAMS (75)
... configuration bitstreams for a programmable **logic** device are disclosed. ...

Method and apparatus for evolving a plurality of versions of a configuration bitstream in parallel
US Pat. 6378122 - Filed Jun 17, 1999 - Xilinx, Inc.
... on a programmable **logic** device In an example embodiment of the invention, ...
configuration bitstreams other chromosomes and other non-**evolvable logic** ...

Method and apparatus for remotely evolving configuration bitstreams
US Pat. 6363517 - Filed Jun 17, 1999 - Xilinx, Inc.
Other chromosomes and other non-**evolvable logic** may also be incorporated in a
... Designs for various other programmable **logic** devices, for example, ...

SYSTEM AND METHOD FOR AUTO-**EVOLVABLE** REMOTE PROCEDURE CALL STRUCTURES BACKGROUND
US Pat. 7100171 - Filed May 10, 2002 - racle International Corp
Second, the application may include **logic** designed to deduce a common set ...
SUMMARY Therefore, in one embodiment of the invention an auto- **evolvable** RFC ...

System, method and article of manufacture for providing an attribute system with primitive support of dynamic and **evolvable** roles in support of fluid and integrative application development
US Pat. 6535884 - Filed Jul 11, 2000 - Xerox Corporation
A system for managing a data item, comprising: (a) **logic** that defines one or more
roles, wherein each role comprises a set of attributes; (b) **logic** that ...

Myoelectric-pattern classification method and apparatus
US Pat. 6859663 - Filed Jan 29, 2002 - National Institute of Advanced Industrial Science and Technology
In pattern classification using the **evolvable** chip, in order to perform classification
by means of the **logic** circuit, classification patterns have to be ...

Evolvable circuit with transistor-level reconfigurability
US Pat. 6728666 - Filed Sep 13, 1999 - The United States of America as represented by the Administrator of the National Aeronautics and Space Administration
"**Evolvable** Hardware or Learning Hardware? Induction of State Machines from Temporal
Logic Constraints" M. Perkowski, ISBN: 0-7695-0256-3, Jul. 1999. ...

Method and apparatus for evolving configuration bitstreams
US Pat. 6430736 - Filed Jun 17, 1999 - Xilinx, Inc.
The process is often 55 characterised as "**evolvable** hardware" or using genetic
... in evolving designs is typically some type of programmable **logic** device. ...

Evolved circuits for bitstream protection
US Pat. 6894527 - Filed May 12, 2003 - Xilinx, Inc.
... al., "On **Evolvable** Hardware,"5o/r Computing in ... Justin Liu; Kim Kanzaki (57)
ABSTRACT A security circuit for a reprogrammable **logic** includes an ...

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evolvable logic Search Patents

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **An extension of ternary majority function and its application to evolvable system**
Yamamoto, Y.;
Multiple-Valued Logic, 2003. Proceedings. 33rd International Symposium on
16-19 May 2003 Page(s):17 - 23
Digital Object Identifier 10.1109/ISMVL.2003.1201379
AbstractPlus | Full Text: PDF(498 KB) **IEEE CNF**
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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **In-situ evolution of a reconfigurable antenna**
Linden, D.S.;
Aerospace Conference, 2001, IEEE Proceedings.
Volume 5, 10-17 March 2001 Page(s):2333 - 2338 vol.5
Digital Object Identifier 10.1109/AERO.2001.931193
AbstractPlus | Full Text: PDF(524 KB) **IEEE CNF**
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Terms used **evolvable logic** Found **46,795** of **193,448**

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Best 200 shown Relevance scale

1 Gate matrix layout of random control logic in a 32-bit CMOS CPU chip adaptable to evolving logic design
S. M. Kang, R. H. Krambeck, H. F. S. Law
January 1982 **Proceedings of the 19th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(560.48 KB) Additional Information: full citation, abstract, references, index terms

Previously the gate matrix technique was used to lay out the RALU section of a CMOS 32-bit CPU chip. It took 1.2 Engineer-Years to complete the layout of the RALU that contained more than 20,000 transistors with multiple-bus structure. The average packing density was 840 &mgr;m2 per transistor in 2.5 &mgr;m design rules. Recently we have applied the gate matrix technique to lay out the highly complex "random control logic" of the CPU. With a well-structured layout strategy, the gate matrix ...

2 Reasoning about evolving nonmonotonic knowledge bases
Thomas Eiter, Michael Fink, Giuliana Sabbatini, Hans Tompits
April 2005 **ACM Transactions on Computational Logic (TOCL)**, Volume 6 Issue 2
Publisher: ACM Press
Full text available: pdf(369.97 KB) Additional Information: full citation, abstract, references, index terms

Recently, several approaches to updating knowledge bases modeled as extended logic programs have been introduced, ranging from basic methods to incorporate (sequences of) sets of rules into a logic program, to more elaborate methods which use an update policy for specifying how updates must be incorporated. In this article, we introduce a framework for reasoning about evolving knowledge bases, which are represented as extended logic programs and maintained by an update policy. We first describe ...

Keywords: Answer-set semantics, computational complexity, knowledge-base evolution, logic-program updates, nonmonotonic knowledge bases, program equivalence, temporal reasoning

3 Genetic programming: papers: A hybridized genetic parallel programming based logic circuit synthesizer
Wai Shing Lau, Kin Hong Lee, Kwong Sak Leung
July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**
Publisher: ACM Press
Full text available: pdf(229.17 KB) Additional Information: full citation, abstract, references, index terms

Genetic Parallel Programming (GPP) is a novel Genetic Programming paradigm. Based on the GPP paradigm and a local search operator - FlowMap, a logic circuit synthesizing

system integrating GPP and FlowMap, a Hybridized GPP based Logic Circuit Synthesizer (HGPPLCS) is developed. To show the effectiveness of the proposed HGPPLCS, six combinational logic circuit problems are used for evaluations. Each problem is run for 50 times. Experimental results show that both the lookup table counts and the p ...

Keywords: FlowMap, LookUp table, a hybridized genetic parallel programming logic circuit synthesizer, field programmable gate array, genetic parallel programming, technology mapping

4 Digital logic simulation models and evolving technology

Cliff W. Hemming, John M. Hemphill

January 1975 **Proceedings of the 12th conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(717.81 KB) Additional Information: full citation, abstract, references, citings, index terms

Digital logic simulators have traditionally served three functions for the designer; those are logic verification, design verification (detailed timing analysis), and fault analysis. Logic verification is well understood and accurate models have existed for this purpose for some time. Design verification has improved steadily over recent years and very accurate models exist for gate-level analysis. Fault analysis has progressed much more slowly, and most models currently used are ...

5 Comparison of access methods for time-evolving data

Betty Salzberg, Vassilis J. Tsotras

June 1999 **ACM Computing Surveys (CSUR)**, Volume 31 Issue 2

Publisher: ACM Press

Full text available: pdf(529.53 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper compares different indexing techniques proposed for supporting efficient access to temporal data. The comparison is based on a collection of important performance criteria, including the space consumed, update processing, and query time for representative queries. The comparison is based on worst-case analysis, hence no assumptions on data distribution or query frequencies are made. When a number of methods have the same asymptotic worst-case behavior, features in the methods tha ...

Keywords: I/O performance, access methods, structures, temporal databases

6 A modal logic for mobile agents

Rocco De Nicola, Michele Loreti

January 2004 **ACM Transactions on Computational Logic (TOCL)**, Volume 5 Issue 1

Publisher: ACM Press

Full text available: pdf(338.36 KB) Additional Information: full citation, abstract, references, index terms

Klaim is an experimental programming language that supports a programming paradigm where both processes and data can be moved across different computing environments. The language relies on the use of explicit localities. This paper presents a temporal logic for specifying properties of Klaim programs. The logic is inspired by Hennessy-Milner Logic (HML) and the μ-calculus, but has novel features that permit dealing with state properties and impact of actions and movements over the different ...

Keywords: Coordination Models, Logics, Mobile Code Languages, Mobility, Proof Systems, Temporal Logics of Programs

7 GA design of crisp-fuzzy logic controllers

Kuan-Shiu Chiu, Andrew Hunter

February 1999 **Proceedings of the 1999 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(549.31 KB) Additional Information: full citation, references, index terms

Keywords: fuzzy logic control, genetic algorithms, real-time control

8 Event choice datalog: a logic programming language for reasoning in multiple dimensions
Gianluigi Greco, Antonella Guzzo, Domenico Saccà, Francesco Scarcello
August 2004 **Proceedings of the 6th ACM SIGPLAN international conference on Principles and practice of declarative programming**
Publisher: ACM Press
Full text available: pdf(307.31 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a rule-based declarative database language which extends DATALOG to express events and nondeterministic state transitions, by using the choice construct to model uncertainty in dynamic rules. The proposed language, called Event Choice DATALOG (DATALOG^{lev} for short), provides a powerful mechanism to formulate queries on the evolution of a knowledge base, given a sequence of events envisioned to occur in the future. A distinguished feature of this language is the use ...

Keywords: knowledge representation, logic programming

9 Special session on reliable computing: Dependability in an evolving world
A. M. Tyrrell
May 2006 **Proceedings of the 3rd conference on Computing frontiers CF '06**
Publisher: ACM Press
Full text available: pdf(1.62 MB) Additional Information: full citation, abstract, references, index terms

Evolvable hardware offers much for the future of complex system design. Evolutionary techniques not only give the potential of larger solution space, but when implemented on hardware allow system designs to adapt to changes in the environment, including failures in system components.This paper reviews a number of techniques, all based in the bio-inspired camp, that provide varying degrees of dependability over and above standard designs. In particular, three different techniques are considered: ...

Keywords: POEtic, evolutionary algorithms, fault-tolerance

10 Propositional computability logic I
Giorgi Japaridze
April 2006 **ACM Transactions on Computational Logic (TOCL)**, Volume 7 Issue 2
Publisher: ACM Press
Full text available: pdf(209.19 KB) Additional Information: full citation, abstract, references, index terms

In the same sense as classical logic is a formal theory of truth, the recently initiated approach called *computability logic* is a formal theory of computability. It understands (interactive) computational problems as games played by a machine against the environment, their computability as existence of a machine that always wins the game, logical operators as operations on computational problems, and validity of a logical formula as being a scheme of "always computabl " proble ...

Keywords: Computability logic, computational resources, game semantics, interactive algorithms, linear logic

11 Logical models of argument

Carlos Iván Chesñevar, Ana Gabriela Maguitman, Ronald Prescott Loui
December 2000 **ACM Computing Surveys (CSUR)**, Volume 32 Issue 4
Publisher: ACM Press

Full text available: pdf(387.16 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Logical models of arguement formalize commonsense reasoning while taking process and computation seriously. This survey discusses the main ideas that characterize different logical models of argument. It presents the formal features of a few features of a few main approaches to the modeling of argumentation. We trace the evolution of argumentation from the mid-1980s, when argument systems emerged as an alternative to nonmonotonic formalisms based on classical logic, to the present, as argum ...

Keywords: argumentation, argumentative systems, defeasible argumentation, defeasible reasoning, reasoning

12 Posters: logical foundations I: A logic of reasoning, communication and cooperation with syntactic knowledge

Thomas Ågotnes, Michal Walicki
July 2005 **Proceedings of the fourth international joint conference on Autonomous agents and multiagent systems AAMAS '05**
Publisher: ACM Press

Full text available: pdf(290.57 KB) Additional Information: full citation, abstract, references, index terms

We present a general logic of explicit knowledge represented as finite sets of logical formulae which can evolve by non-deterministic reasoning and communication. It is partly based on Alternating-time Temporal Logic, which allows the expression of properties of cooperation. Properties of an agent's reasoning mechanism such as "the agent knows modus ponens" can be expressed. Instead of a common closure condition such as "if the agent knows both p and $p \rightarrow q$, he must also ...

Keywords: ATL, epistemic logic, syntactic knowledge representation

13 Extensionality and intensionality of the ambient logics

Davide Sangiorgi
January 2001 **ACM SIGPLAN Notices , Proceedings of the 28th ACM SIGPLAN-SIGACT symposium on Principles of programming languages POPL '01**, Volume 36 Issue 3
Publisher: ACM Press

Full text available: pdf(750.57 KB) Additional Information: full citation, abstract, references, citings, index terms

The *ambient logic* has been proposed for expressing properties of process mobility in the calculus of Mobile Ambients (MA), and as a basis for query languages on semistructured data. To understand the extensionality and the intensionality of the logic, the equivalence on MA processes induced by the logic (=L) iscompared with the standard MA behavioural equivalence and with structural congruence (an intensional equivalence, used as an auxiliary relation in thedefinition ...

14 Object-oriented logical specification of time-critical systems

Angelo Morzenti, Pierluigi San Pietro
January 1994 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 3 Issue 1
Publisher: ACM Press

Full text available: pdf(3.05 MB) Additional Information: full citation, abstract, references, citings, index terms, review

We define TRIO+, an object-oriented logical language for modular system specification. TRIO+ is based on TRIO, a first-order temporal language that is well suited to the

specification of embedded and real-time systems, and that provides an effective support to a variety of validation activities, like specification testing, simulation, and property proof. Unfortunately, TRIO lacks the ability to construct specifications of complex systems in a system ...

Keywords: first-order logic, formal specifications, model-theoretic semantics, object-oriented methodologies, real-time systems, temporal logic

15 Cooperating evolving components: a rigorous approach to evolving large software systems

R. M. Greenwood, B. C. Warboys, J. Sa

May 1996 **Proceedings of the 18th international conference on Software engineering**

Publisher: IEEE Computer Society

Full text available: pdf(975.98 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Large software systems have a large number of components and are developed over a long time period frequently by a large number of people. We describe a framework approach to evolving such systems based on an integration of product and process modelling. The evolving system is represented as a Product Tower, a hierarchy of components which provides views of the product at multiple levels of refinement. The evolution process is component based with the cooperation between components being mediate ...

Keywords: design hierarchy, process evolution, process modelling, product evolution

16 Treating coordination in logic grammars

Veronica Dahl, Michael C. McCord

April 1983 **Computational Linguistics**, Volume 9 Issue 2

Publisher: MIT Press

Full text available: pdf(1.58 MB) Publisher Site Additional Information: full citation, abstract, references, citings

Logic grammars are grammars expressible in predicate logic. Implemented in the programming language Prolog, logic grammar systems have proved to be a good basis for natural language processing. One of the most difficult constructions for natural language grammars to treat is coordination (construction with conjunctions like 'and'). This paper describes a logic grammar formalism, *modifier structure grammars* (MSGs), together with an interpreter written in Prolog, which can handle coordinati ...

17 Supporting communication between designers with artifact-centered evolving information spaces

Brent Reeves, Frank Shipman

December 1992 **Proceedings of the 1992 ACM conference on Computer-supported cooperative work**

Publisher: ACM Press

Full text available: pdf(883.45 KB) Additional Information: full citation, references, citings, index terms

Keywords: artifact based communication, asynchronous collaboration, design environments, information spaces

18 Human-computer interface development: concepts and systems for its management

H. Rex Hartson, Deborah Hix

March 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 1

Publisher: ACM Press

Full text available: pdf(7.97 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Human-computer interface management, from a computer science viewpoint, focuses on the process of developing quality human-computer interfaces, including their representation, design, implementation, execution, evaluation, and maintenance. This survey presents important concepts of interface management: dialogue independence, structural modeling, representation, interactive tools, rapid prototyping, development methodologies, and control structures. *Dialogue independence* is th ...

19 The evolution of the DECsystem 10

C. G. Bell, A. Kotok, T. N. Hastings, R. Hill
January 1978 **Communications of the ACM**, Volume 21 Issue 1

Publisher: ACM Press

Full text available: pdf(1.92 MB) Additional Information: full citation, abstract, references, citings, index terms

The DECsystem 10, also known as the PDP-10, evolved from the PDP-6 (circa 1963) over five generations of implementations to presently include systems covering a price range of five to one. The origin and evolution of the hardware, operating system, and languages are described in terms of technological change, user requirements, and user developments. The PDP-10's contributions to computing technology include: accelerating the transition from batch oriented to time sharing computing systems; ...

Keywords: architecture, computer structures, operating system, timesharing

20 Probabilistic logic programming with conditional constraints

Thomas Lukasiewicz
July 2001 **ACM Transactions on Computational Logic (TOCL)**, Volume 2 Issue 3

Publisher: ACM Press

Full text available: pdf(894.45 KB) Additional Information: full citation, abstract, references, citings, index terms

We introduce a new approach to probabilistic logic programming in which probabilities are defined over a set of possible worlds. More precisely, classical program clauses are extended by a subinterval of [0,1] that describes a range for the conditional probability of the head of a clause given its body. We then analyze the complexity of selected probabilistic logic programming tasks. It turns out that probabilistic logic programming is computationally more complex than classical logic progr ...

Keywords: computational complexity, conditional constraint, logic programming, many-valued logic, probabilistic logic, probabilistic logic programming, probabilistic reasoning, probability, quantitative deduction, uncertainty

Terms used **evolvable circuit** Found **28,073** of **193,448**

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1 Special session on reliable computing: On dependability of FPGA-based evolvable hardware systems that utilize virtual reconfigurable circuits
Lukas Sekanina
May 2006 **Proceedings of the 3rd conference on Computing frontiers CF '06**
Publisher: ACM Press
Full text available: pdf(179.75 KB) Additional Information: full citation, abstract, references, index terms

This paper describes experiments conducted to estimate how the use of (area-demanding) virtual reconfigurable circuits (VRC) influences the dependability of FPGA-based evolvable systems. It is shown that these systems are not so sensitive to faults as their area-demanding implementations could evoke. Evolutionary techniques are utilized to design fault tolerant circuits in a virtual reconfigurable circuit and to perform their automatic functional recovery in case of occurence of faults in a conf ...

Keywords: FPGA, dependability, evolutionary algorithms, evolvable hardware

2 Experiments on evolving software models of analog circuits
Jason D. Lohn
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(157.15 KB) html(13.21 KB) Additional Information: full citation, references, index terms

3 Genetic programming: papers: A hybridized genetic parallel programming based logic circuit synthesizer
Wai Shing Lau, Kin Hong Lee, Kwong Sak Leung
July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**
Publisher: ACM Press
Full text available: pdf(229.17 KB) Additional Information: full citation, abstract, references, index terms

Genetic Parallel Programming (GPP) is a novel Genetic Programming paradigm. Based on the GPP paradigm and a local search operator - FlowMap, a logic circuit synthesizing system integrating GPP and FlowMap, a Hybridized GPP based Logic Circuit Synthesizer (HGPPLCS) is developed. To show the effectiveness of the proposed HGPPLCS, six combinational logic circuit problems are used for evaluations. Each problem is run for 50 times. Experimental results show that both the lookup table counts and the p ...

Keywords: FlowMap, LookUp table, a hybridized genetic parallel programming logic

circuit synthesizer, field programmable gate array, genetic parallel programming, technology mapping

4 Evolvable hardware: papers: Evolutionary design of fault-tolerant analog control for a piezoelectric pipe-crawling robot

Geoffrey A. Hollinger, David A. Gwaltney

July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**

Publisher: ACM Press

Full text available: pdf(418.13 KB) Additional Information: full citation, abstract, references, index terms

In this paper, a genetic algorithm (GA) is used to design fault-tolerant analog controllers for a piezoelectric micro-robot. First-order and second-order functions are developed to model the robot's piezoelectric actuators, and the GA is used to evolve closed-loop controllers for both models. The GA is first used to assist in traditional PID design and is later used to synthesize variable topology analog controllers. Through the use of a compact circuit representation, runtimes are minimized and ...

Keywords: evolvable hardware, genetic algorithms, inspection robots, piezoelectric actuators, robot control

5 SEEDS contributions: Providing information from the environment for growing electronic circuits through polymorphic gates

Michal Bidlo, Lukas Sekanina

June 2005 **Proceedings of the 2005 workshops on Genetic and evolutionary computation GECCO '05**

Publisher: ACM Press

Full text available: pdf(211.42 KB) Additional Information: full citation, abstract, references, index terms

This paper deals with the evolutionary design of programs (constructors) that are able to create (n+2)-input circuits from n-input circuits. The growing circuits are composed of polymorphic gates considered as building blocks. Therefore, the growing circuit can specialize its functionality according to environment which is sensed through polymorphic gates. The work was performed using a simple circuit simulator. We evolved constructors that are able to create arbitrarily large poly ...

Keywords: development, digital circuits design, genetic algorithm, polymorphic circuit

6 Analysis of unconventional evolved electronics

Adrian Thompson, Paul Layzell

April 1999 **Communications of the ACM**, Volume 42 Issue 4

Publisher: ACM Press

Full text available: pdf(255.72 KB) html(37.68 KB) Additional Information: full citation, references, citings, index terms

7 Evolving effective CA/CSTP: BIST architectures for sequential circuits

F. Corno, M. Sonza Reorda, G. Squillero

March 2001 **Proceedings of the 2001 ACM symposium on Applied computing**

Publisher: ACM Press

Full text available: pdf(66.11 KB) Additional Information: full citation, references, index terms

8 Special session on reliable computing: Dependability in an evolving world

A. M. Tyrrell

May 2006 **Proceedings of the 3rd conference on Computing frontiers CF '06**
Publisher: ACM Press
Full text available: pdf(1.62 MB) Additional Information: full citation, abstract, references, index terms

Evolvable hardware offers much for the future of complex system design. Evolutionary techniques not only give the potential of larger solution space, but when implemented on hardware allow system designs to adapt to changes in the environment, including failures in system components.This paper reviews a number of techniques, all based in the bio-inspired camp, that provide varying degrees of dependability over and above standard designs. In particular, three different techniques are considered: ...

Keywords: POEtic, evolutionary algorithms, fault-tolerance

9 Evolvable hardware: papers: Filter approximation using explicit time and frequency domain specifications
Varun Aggarwal, Wesley O Jin, Una-May O'Reilly
July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**
Publisher: ACM Press
Full text available: pdf(227.40 KB) Additional Information: full citation, abstract, references, index terms

We demonstrate that particle swarm optimization (PSO) can be successfully used to evolve high performance filter approximations. These evolved approximations use sets of quantitative specifications which conventional analytically derived approximations can not directly employ. The conventional derivations use only a subset of the quantitative specifications in their algorithm and the remaining specifications are side-effect results of the algorithm. Thus, with PSO, instead of a filter designer h ...

Keywords: filter design, particle swarm optimization

10 Evolvable hardware chips for industrial applications
Tetsuya Higuchi, Nobuki Kajihara
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(398.72 KB) html(25.20 KB) Additional Information: full citation, references, citings, index terms, review

11 Following the path of evolvable hardware
Xin Yao
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(165.68 KB) html(11.87 KB) Additional Information: full citation, references, citings, index terms

12 Genetic programming: Evolution of a human-competitive quantum fourier transform algorithm using genetic programming
Paul Massey, John A. Clark, Susan Stepney
June 2005 **Proceedings of the 2005 conference on Genetic and evolutionary computation GECCO '05**
Publisher: ACM Press
Full text available: pdf(280.68 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we show how genetic programming (GP) can be used to evolve system-size-independent quantum algorithms, and present a human-competitive Quantum

Fourier Transform (QFT) algorithm evolved by GP.

Keywords: evolutionary computing, genetic algorithms, genetic programming, quantum computing, quantum fourier transform

13 Evolutionary discovery of algorithms as circuits for quantum computers

Alvin J. Surkan, Amiran Khuskivadze
June 2002 **ACM SIGAPL APL Quote Quad , Proceedings of the 2002 conference on APL: array processing languages: lore, problems, and applications APL '02**, Volume 32 Issue 4
Publisher: ACM Press
Full text available: pdf(113.30 KB) Additional Information: full citation, abstract, references

This paper demonstrates an application of an evolutionary approach for solving a class of non-trivial, hardware-design problems. Array processing features of the computer language APL simplify the implementation of an evolutionary solution in which simulation is performed by a genetic algorithm on a population of candidate solutions until one or more are satisfactory quantum algorithms. The objective of the simulation model is the automatic discovery of quantum computer algorithms. The algorithm ...

14 Evolution using genetic programming of a low-distortion, 96 decibel operational amplifier

John R. Koza, Forrest H. Bennett, David Andre, Martin A. Keane
April 1997 **Proceedings of the 1997 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(913.91 KB) Additional Information: full citation, references, index terms

Keywords: analog circuit synthesis, automated circuit design, genetic programming, operational amplifier

15 Sequential circuit test generation in a genetic algorithm framework

Elizabeth M. Rudnick, Janak H. Patel, Gary S. Greenstein, Thomas M. Niermann
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(181.69 KB) Additional Information: full citation, references, citings, index terms

16 Session 1: Applications: New directions for integrated circuit cards operating systems

Pierre Paradinas, Jean-Jacques Vandewalle
September 1994 **Proceedings of the 6th workshop on ACM SIGOPS European workshop: Matching operating systems to application needs**
Publisher: ACM Press
Full text available: pdf(437.96 KB) Additional Information: full citation, abstract, references

Integrated circuit cards or smart cards are now well-known. Applications such as electronic purses (cash units stored in cards), subscriber identification cards used in cellular telephone or access keys for pay-TV and information highways emerge in many places with millions of users. More services are required by applications providers and card holders. Mainly, new integrated circuit cards evolve towards non-predefined multi-purpose, open and multi-user applications. Today, operating systems imp ...

Keywords: Integrated Circuit Card Applications, Integrated Circuit Card Operating System, Object-Oriented Technologies, Secured method execution

17 New directions for integrated circuit cards operating systems

Pierre Paradinas, Jean-Jacques Vandewalle
January 1995 **ACM SIGOPS Operating Systems Review**, Volume 29 Issue 1
Publisher: ACM Press
Full text available: pdf(422.64 KB) Additional Information: full citation, abstract, index terms

Integrated circuit cards or smart cards are now well-known. Applications such as electronic purses (cash units stored in cards), subscriber identification cards used in cellular telephone or access keys for pay-TV and information highways emerge in many places with millions of users. More services are required by applications providers and card holders. Mainly, new integrated circuit cards evolve towards non-predefined multi-purpose, open and multi-user applications. Today, operating systems imp ...

Keywords: integrated circuit card applications, integrated circuit card operating system, object-oriented technologies, secured method execution

18 ASTRX/OBLX: tools for rapid synthesis of high-performance analog circuits

Emil S. Ochotta, Rob A. Rutenbar, L. Richard Carley
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(98.20 KB) Additional Information: full citation, references, citings, index terms

19 A Framework for Designing Reusable Analog Circuits

Dean Liu, Stefanos Sidiropoulos, Mark Horowitz
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(262.75 KB) Additional Information: full citation, abstract, index terms

Recent analog design tools have started to allow designers to archivenot only the sized schematics but also some of the objectives thatthe circuit is trying to achieve. This paper first describes STAR(Schematic Tool for Analog Reuse), a system that captures designer'sknowledge as part of the archival circuit representation,and then describes how this system can be used to create portabledesign modules. Creating portable analog modules require morethan just the optimization criteria for the cell. ...

20 Device-level early floorplanning algorithms for RF circuits

Mehmet Aktuna, Rob A. Rutenbar, L. Richard Carley
April 1998 **Proceedings of the 1998 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

High-frequency circuits are notoriously difficult to lay out because of the tight coupling between device-level placement and wiring. Given that successful electrical performance requires careful control of the lowest-level geometric features—wire bends, precise length, proximity, planarity, etc.—we suggest a new layout strategy for these circuits: early floorplanning at the device level. This paper develops a floorplanner for RF circuits based on a genetic algorithm (GA) that s ...

Terms used **evolvable circuit** and **chromosomes** Found **5,086** of **193,448**

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1 Special session on reliable computing: On dependability of FPGA-based evolvable hardware systems that utilize virtual reconfigurable circuits
Lukas Sekanina
May 2006 **Proceedings of the 3rd conference on Computing frontiers CF '06**
Publisher: ACM Press
Full text available: pdf(179.75 KB) Additional Information: full citation, abstract, references, index terms

This paper describes experiments conducted to estimate how the use of (area-demanding) virtual reconfigurable circuits (VRC) influences the dependability of FPGA-based evolvable systems. It is shown that these systems are not so sensitive to faults as their area-demanding implementations could evoke. Evolutionary techniques are utilized to design fault tolerant circuits in a virtual reconfigurable circuit and to perform their automatic functional recovery in case of occurence of faults in a conf ...

Keywords: FPGA, dependability, evolutionary algorithms, evolvable hardware

2 Genetic programming: papers: A multi-chromosome approach to standard and embedded cartesian genetic programming
James Alfred Walker, Julian Francis Miller, Rachel Cavill
July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**
Publisher: ACM Press
Full text available: pdf(190.73 KB) Additional Information: full citation, abstract, references, index terms

Embedded Cartesian Genetic Programming (ECGP) is an extension of Cartesian Genetic Programming (CGP) that can automatically acquire, evolve and re-use partial solutions in the form of modules. In this paper, we introduce for the first time a new multi-chromosome approach to CGP and ECGP that allows difficult problems with multiple outputs to be broken down into many smaller, simpler problems with single outputs, whilst still encoding the entire solution in a single genotype. We also propose a mu ...

Keywords: automatically defined functions, cartesian genetic programming, digital circuits, embedded cartesian genetic programming, evolution, module acquisition, multi-chromosome, multi-chromosome evolutionary strategy

3 Following the path of evolvable hardware
Xin Yao
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press

Full text available: pdf(165.68 KB) html(11.87 KB) Additional Information: full citation, references, citings, index terms

4 SEEDS contributions: Providing information from the environment for growing electronic circuits through polymorphic gates

Michal Bidlo, Lukas Sekanina

June 2005 **Proceedings of the 2005 workshops on Genetic and evolutionary computation GECCO '05**

Publisher: ACM Press

Full text available: pdf(211.42 KB) Additional Information: full citation, abstract, references, index terms

This paper deals with the evolutionary design of programs (constructors) that are able to create (n+2)-input circuits from n-input circuits. The growing circuits are composed of polymorphic gates considered as building blocks. Therefore, the growing circuit can specialize its functionality according to environment which is sensed through polymorphic gates. The work was performed using a simple circuit simulator. We evolved constructors that are able to create arbitrarily large poly ...

Keywords: development, digital circuits design, genetic algorithm, polymorphic circuit

5 Evolvable hardware chips for industrial applications

Tetsuya Higuchi, Nobuki Kajihara

April 1999 **Communications of the ACM**, Volume 42 Issue 4

Publisher: ACM Press

Full text available: pdf(398.72 KB) html(25.20 KB) Additional Information: full citation, references, citings, index terms, review

6 Real-world applications: papers: Evolution of driving agent, remotely operating a scale model of a car with obstacle avoidance capabilities

Ivan Tanev, Michal Joachimczak, Katsunori Shimohara

July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**

Publisher: ACM Press

Full text available: pdf(783.43 KB) Additional Information: full citation, abstract, references, index terms

We present an approach for evolutionary design of an agent, remotely operating a scale model of a car running in a fastest possible way. The agent perceives the environment from a video camera and conveys its actions to the car via standard radio control transmitter. In order to cope with the video feed latency we propose an anticipatory modeling in which the agent considers its current actions based on the anticipated intrinsic (rather than currently available, outdated) state of the car and it ...

Keywords: anticipatory modeling, driving agent, feedback latency, genetic algorithms

7 Test (co-organized with LA-TTTC): ATPG for fault diagnosis on analog electrical networks using evolutionary techniques

C. E. F. Savioli, C. E. C. Szendrodi, J. V. Calvano, A. C. Mesquita

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Publisher: ACM Press

Full text available: pdf(192.74 KB) Additional Information: full citation, abstract, references, index terms

This paper proposes a method for automated test pattern generation for fault diagnosis on continuous-time analog electrical networks based on evolutionary techniques. The paper states a method for coding a generic algorithm, based on a given heuristic, that are

able to generate a set of optimum frequencies capable to disclose parametric faults. The method itself is generic, and not based on specific or ad hoc features at all.

Keywords: analog and mixed-signal test, automatic test pattern generation, fault models, genetic algorithms

8 A fast and stable hybrid genetic algorithm for the ratio-cut partitioning problem on hypergraphs
Thang Nguyen Bui, Byung Ro Moon
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(218.09 KB) Additional Information: full citation, references, citings, index terms

9 Evolutionary discovery of algorithms as circuits for quantum computers
Alvin J. Surkan, Amiran Khuskivadze
June 2002 **ACM SIGAPL APL Quote Quad , Proceedings of the 2002 conference on APL: array processing languages: lore, problems, and applications APL '02**, Volume 32 Issue 4
Publisher: ACM Press
Full text available: pdf(113.30 KB) Additional Information: full citation, abstract, references

This paper demonstrates an application of an evolutionary approach for solving a class of non-trivial, hardware-design problems. Array processing features of the computer language APL simplify the implementation of an evolutionary solution in which simulation is performed by a genetic algorithm on a population of candidate solutions until one or more are satisfactory quantum algorithms. The objective of the simulation model is the automatic discovery of quantum computer algorithms. The algorithm ...

10 Sequential circuit test generation in a genetic algorithm framework
Elizabeth M. Rudnick, Janak H. Patel, Gary S. Greenstein, Thomas M. Niermann
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(181.69 KB) Additional Information: full citation, references, citings, index terms

11 Hardware evolution system AdAM
Tomofumi Hikage, Hitoshi Hemmi, Katsunori Shimohara
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(173.57 KB) html(8.14 KB) Additional Information: full citation, references, index terms

12 Computational Intelligence Characterization Method of Semiconductor Device
Eric Liau, Doris Schmitt-Landsiedel
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '05**
Publisher: IEEE Computer Society
Full text available: pdf(134.02 KB) Additional Information: full citation, abstract, index terms

Characterization of semiconductor devices is used to gather as much data about the device as possible to determine weaknesses in design or trends in the manufacturing process. In this paper, we propose a novel multiple trip point characterization concept to overcome the constraint of single trip point concept in device characterization phase. In addition, we use computational intelligence techniques (e.g. neural network, fuzzy and

genetic algorithm) to further manipulate these sets of multiple t ...

13 Special session on reliable computing: Dependability in an evolving world

A. M. Tyrrell
May 2006 **Proceedings of the 3rd conference on Computing frontiers CF '06**
Publisher: ACM Press
Full text available: pdf(1.62 MB) Additional Information: full citation, abstract, references, index terms

Evolvable hardware offers much for the future of complex system design. Evolutionary techniques not only give the potential of larger solution space, but when implemented on hardware allow system designs to adapt to changes in the environment, including failures in system components.This paper reviews a number of techniques, all based in the bio-inspired camp, that provide varying degrees of dependability over and above standard designs. In particular, three different techniques are considered: ...

Keywords: POEtic, evolutionary algorithms, fault-tolerance

14 Sequential Circuit Test Generation Using Dynamic State Traversal

Michael S. Hsiao, Elizabeth M. Rudnick, Janak H. Patel
March 1997 **Proceedings of the 1997 European conference on Design and Test**
Publisher: IEEE Computer Society
Full text available: pdf(925.92 KB) Publisher Site Additional Information: full citation, abstract, citings

This research was supported in part by the Semiconductor Research Corporation under contract SRC 96-DP-109, in part by ARPA under contract DABT63-95-C-0069, and by Hewlett-Packard under an equipment grant. A new method for state justification is proposed for sequential circuit test generation. The linear list of states dynamically obtained during the derivation of test vectors is used to guide the search during state justification. State-transfer sequences may already be known that drive the cir ...

Keywords: test generation, genetic algorithms, state-transfer, state justification, genetic engineering

15 The application of genetic algorithms to the design of reconfigurable reasoning VLSI chips

Moritoshi Yasunaga, Jung Hwan Kim, Ikuo Yoshihara
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(672.51 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present a new genetic-algorithm-based design methodology for reasoning VLSI chips, called as LoDETT (logic design with the evolved truth table). In LoDETT, each task's case database is transformed into truth tables, which are evolved to obtain generalization capability (i.e. rules behind the past cases) through genetic algorithms. Digital circuits are synthesized from the evolved truth-tables. Parallelism in each task can be embedded directly in the circuits by the direct ...

16 Genetic VLSI circuit partitioning with two-dimensional geographic crossover and zigzag mapping

Buyng-Ro Moon, Yoon-Sik Lee, Chun-Kyung Kim
April 1997 **Proceedings of the 1997 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(499.27 KB) Additional Information: full citation, references, index terms

Keywords: circuit partitioning, equivalence class, genetic algorithm, geographic crossover, geographical linkage

17 GATutor: a graphical tutorial system for genetic algorithms

Charles Prince, Roger L. Wainwright, Dale A. Schoenefeld, Travis Tull
March 1994 **ACM SIGCSE Bulletin , Proceedings of the twenty-fifth SIGCSE symposium on Computer science education SIGCSE '94**, Volume 26 Issue 1
Publisher: ACM Press

Full text available: pdf(761.77 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we discuss the design and implementation of GATutor, a graphical tutorial system for genetic algorithms (GA). The X Window/Motif system provides powerful tools for the development of a user interfaces with a familiar feel and look. We implemented the Traveling Salesman Problem (TSP) and the Set Covering Problem (SCP) as two example GA problems in the tutorial. The TSP problem uses an order-based chromosome representation (permutation of n objects), while the S ...

18 Dynamic state traversal for sequential circuit test generation

Michael S. Hsiao, Elizabeth M. Rudnick, Janak H. Patel
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3
Publisher: ACM Press

Full text available: pdf(138.10 KB) Additional Information: full citation, abstract, references, citings, index terms

A new method for state justification is proposed for sequential circuit test generation. The linear list of states dynamically obtained during the derivation of test vectors is used to guide the search during state justification. State-transfer sequences that drive the circuit from the current state to the target state may already be known. Otherwise, genetic engineering of existing state-transfer sequences is required. In both cases, genetic-algorithm-based techniques are ...

Keywords: automatic test pattern generation (ATPG), finite-state-machine traversal, genetic algorithms, sequential circuits, simulation-based, testing

19 Special issue on SAC 2001 best papers: Evolutionary image enhancement with user behavior modeling

Cristian Munteanu, Agostinho Rosa
April 2001 **ACM SIGAPP Applied Computing Review**, Volume 9 Issue 1
Publisher: ACM Press
Full text available: pdf(831.87 KB) Additional Information: full citation, abstract, references

In this paper we present a novel method for image enhancement of gray-scale images based on the simulation of evolution. Our method employs Genetic Algorithms to evolve the shape of the contrast curve in the image, while attempting to partially automate the subjective process of image evaluation (e.g. user behavior) by performing multiple regression on fitness values. Results obtained show the robustness and efficiency of the evolutive method for image enhancement. For several images in the test ...

Keywords: image enhancement, multiple regression, real-coded genetic algorithms, subjective fitness

20 Evolutionary image enhancement with user behaviour modeling

Cristian Munteanu, Agostinho Rosa
March 2001 **Proceedings of the 2001 ACM symposium on Applied computing**
Publisher: ACM Press

Keywords: image enhancement, multiple regression, real-coded genetic algorithms, subjective fitness

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L8	8	"716".clas. and evolv$6 same circuit same chromosomes	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/21 15:21
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